

**ASSIGNMENT 6**

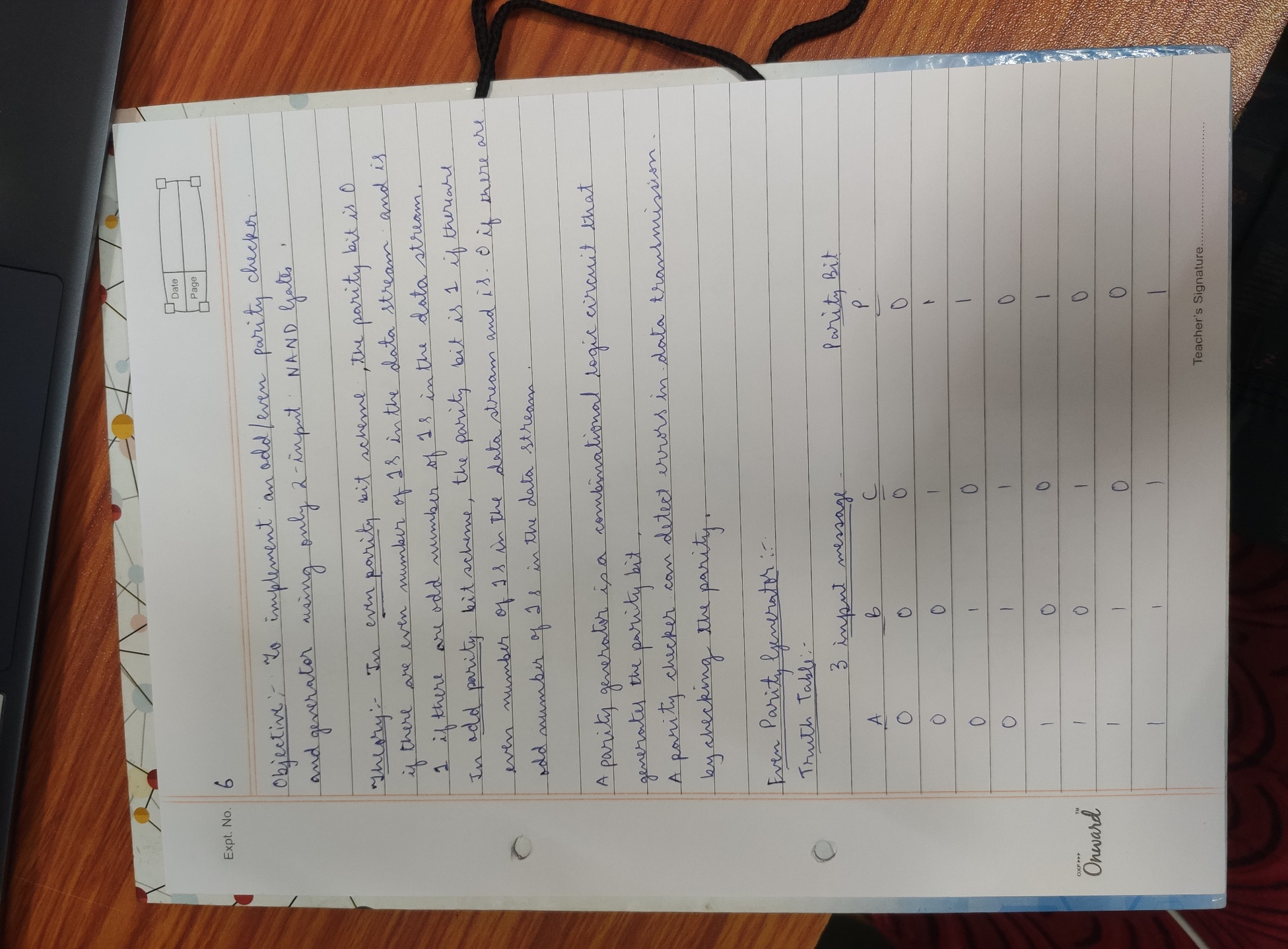
[Design of a combinational logic circuit for **ODD/EVEN PARITY GENERATOR AND CHECKER** using 2 input NAND GATES]

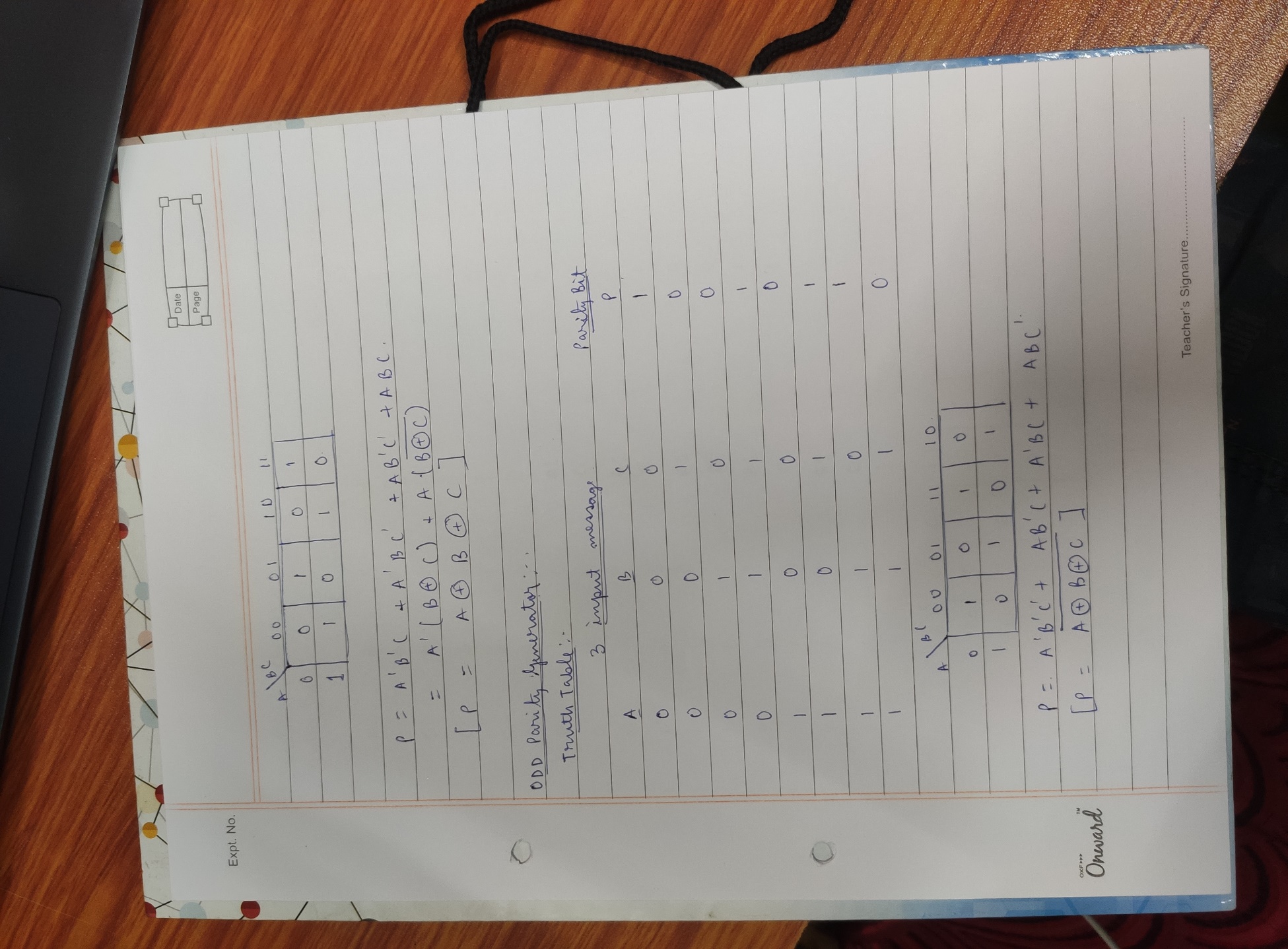


**NAME: ROHIT SADHU**

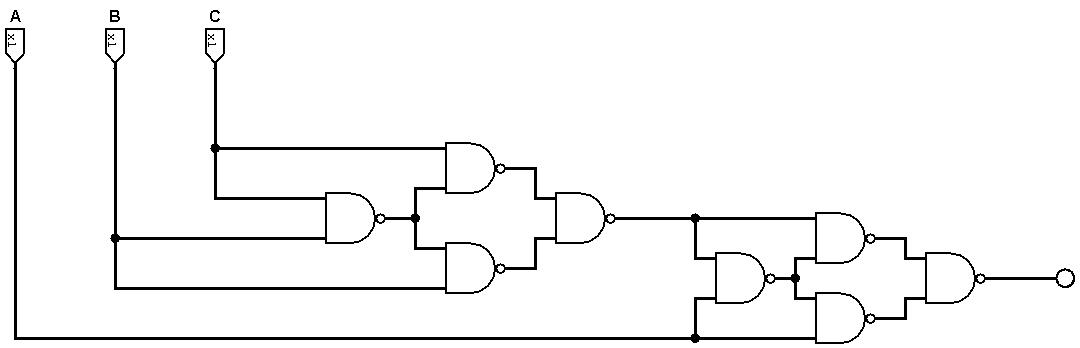
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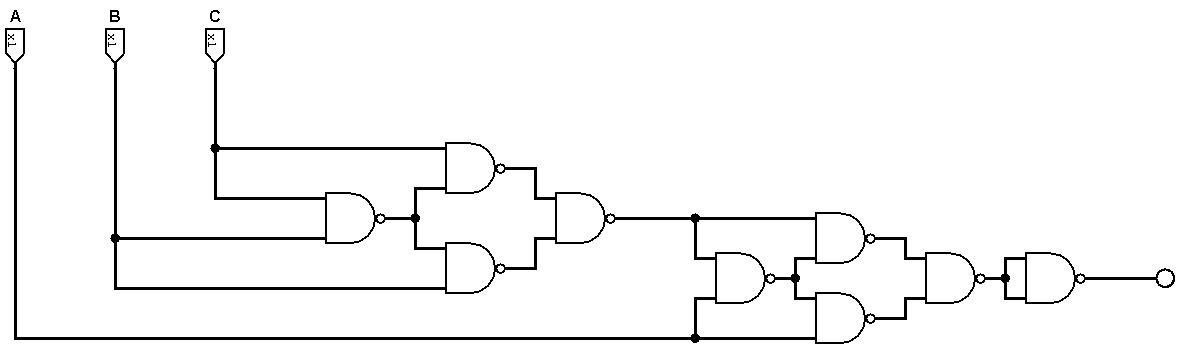


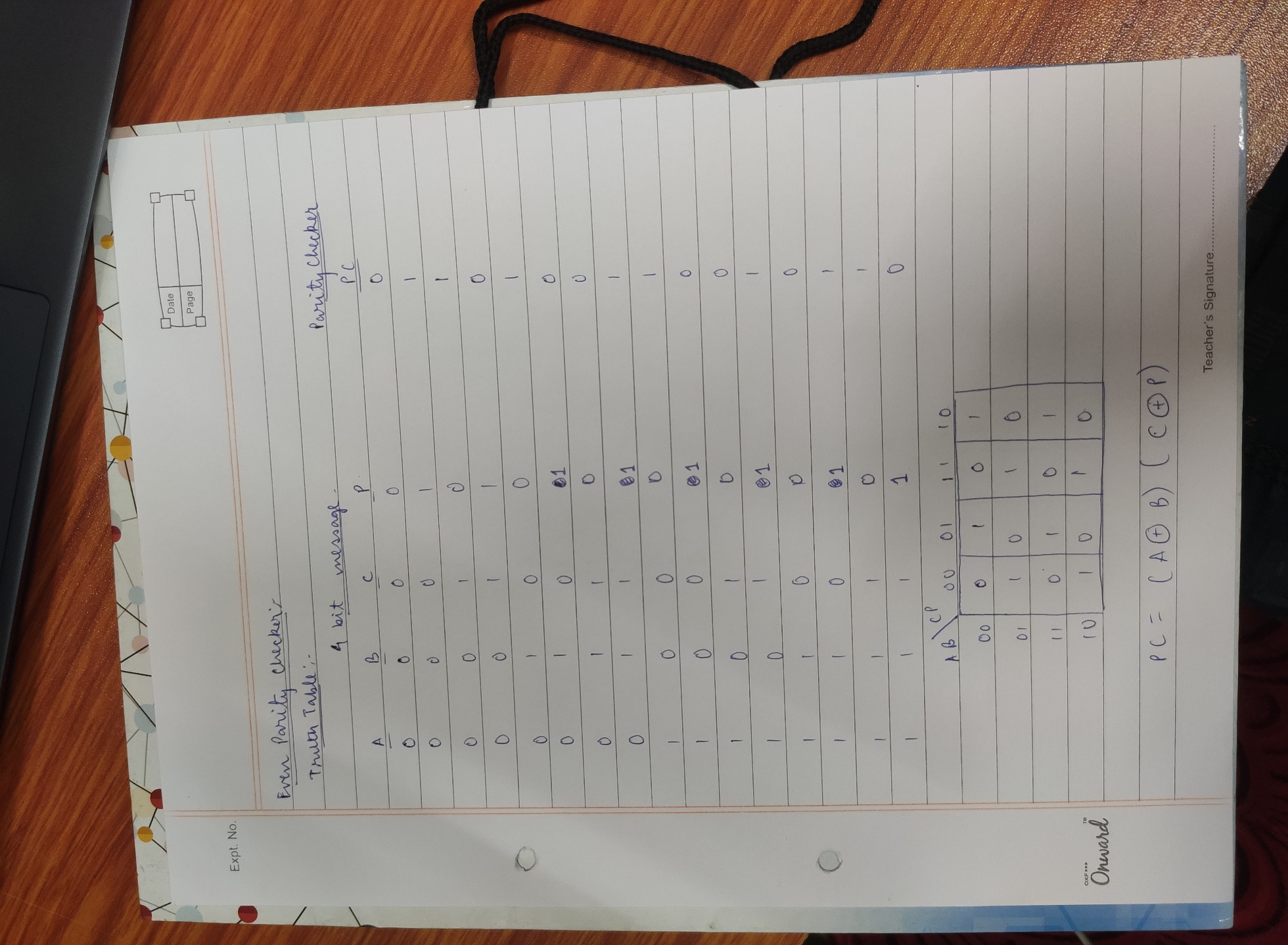


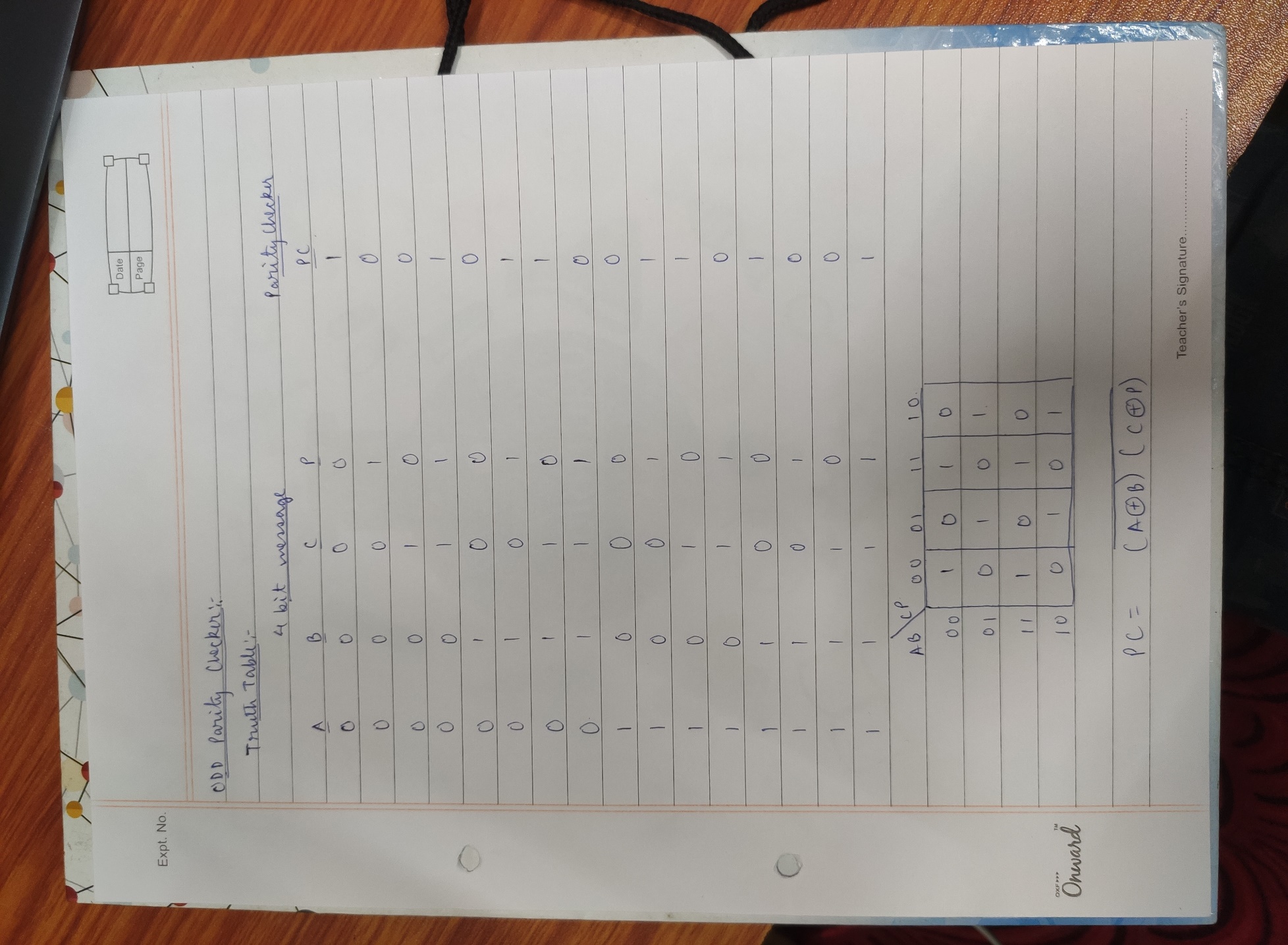
**CIRCUIT DIAGRAM:**

**EVEN PARITY GENERATOR:**

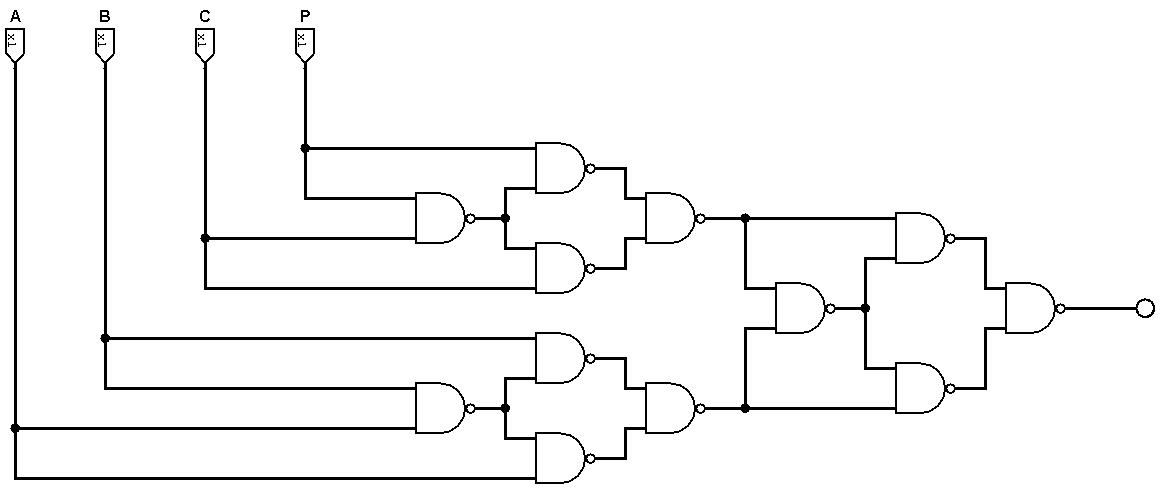
**ODD PARITY GENERATOR:**

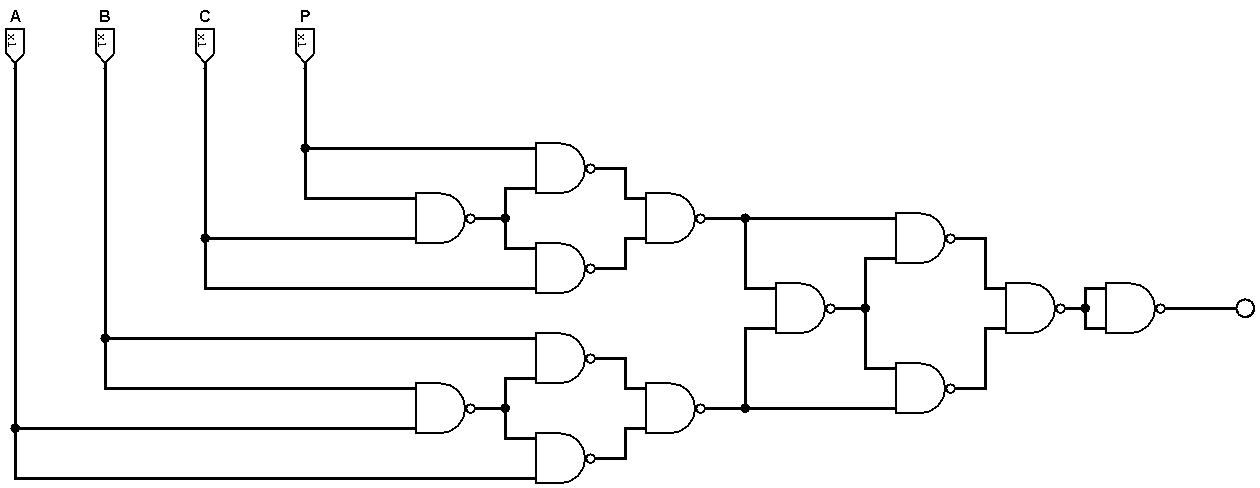






**CIRCUIT DIAGRAM:**

**EVEN PARITY CHECKER:**

**ODD PARITY CHECKER:**